Design-Level Assessment of Overlay Impact Across DPL Technology Options

Motivation
- Double patterning lithography introduces additional variability in linewidth and space
- Different DPL technology options (process methods, resist types, critical features, etc.) have different impacts on linewidth and space
  Different capacitance and resistance variation, and different impact on timing

2009 Main Objectives
- Analysis of mechanisms of interconnect (BEOL) variation in DPL across various technology options.
- Development of design-level analysis framework considering additional variability in DPL, based on commercial tool sets
- Assessment of design level impacts of BEOL variations (width/space) across DPL technology options using our framework
  - Capacitance variation
  - Crosstalk delay variation
  - Total negative slack variation

The Problem
- Need for quantified analyses of various DPL technology options
  - Impact on linewidth and space variation is different according to DPL options
  - Controllability of CD and overlay is different according to DPL options
- Need for automated design-level assessment methodologies and frameworks
- Need for guidance to designers and lithographers to choose the best DPL options for their purposes considering the cost of DPL options

Scenarios
- We analyze linewidth and space variation across various DPL technology options
- 6 different scenarios

Variations in DE/DP
- Double exposure / double patterning
  - Variation caused by overlay error between two lithography steps
  - Width OR space variation

Variations in SDP
- Spacer double patterning
  - Variation caused by spacer thickness variation
  - Width AND space variation

Design-Level Analysis Framework
- We analyze interconnect variations due to overlay and spacer thickness variations in DPL
- We provide a design-level analysis framework considering additional variability in DPL technology options for entire full-chip timing including FEOL variations in DPL
- We seek full analysis / comparison framework across technology options for DPL, based on commercial tool sets
- We also seek development of timing analysis and optimization methodology, incorporated with statistical techniques to target pessimism reduction

Maximum Crosstalk-Induced Delay
- SDP shows more sensitivity -> tighter spacer thickness control spec
- P-DE/DP shows least sensitivity -> looser overlay spec

Summary of Observations
- Capacitance can vary more than 10% due to misalignment
- Timing can be degraded significantly, more than 10% worse TNS
- With the same 3σ variation spec (12nm) for all DPL options, P-DE/DP may be the most favorable option for BEOL DPL
- Overlap control spec for P-DE/DP can be relaxed by 2X compared to others
- With different variation spec, e.g., 3σ for DE/DP, and 1σ for SDP, Amount of impact can be similar to each other
- Need to consider design and lithographic cost
- In each DE/DP or SDP, positive type (P-DE/DP, or P-SDP) has smaller impact on design

Future Goals
- We provide a design-level interconnect analysis framework for double patterning lithography
  - We analyze interconnect variations due to overlay and spacer thickness variation in DPL
  - We compare the impact of interconnect variations across various DPL options
- We seek full analysis / comparison framework across technology options for entire full-chip timing including FEOL variations in DPL
- We also seek development of timing analysis and optimization methodology, incorporated with statistical techniques to target pessimism reduction

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