Motivation

- Process variations from lithography, etch, and CMP affect interconnect width, sidewall angle, and height.
- As physical wire dimensions decrease with scaling, the impact of process variations will be more severe.
- Pattern-Matcher is a fast-CAD tool that can be used to identify layout geometries sensitive to non-idealities in fabrication.
- Leverage speed of Pattern Matching to compensate for physical variations in design flows.

2007 Main Objectives

- **Prototype Pattern-Matching for predicting interconnect delay variation (LITH Y3.5)**
  - Develop maximum likelihood functions and netlist tracking software for quantifying and summing variations in interconnect delay due to residual process nonidealities.
- **Demonstrate accuracy and speed of Pattern-Matching for predicting interconnect delay variation (LITH Y4.5)**
  - Compare Pattern Matching estimates of interconnect delay variation including full chip CMP modeling with brute force modeling.

The Problem

- Parasitic resistance and capacitance extraction is done at two corners of wire width and thickness.
- Variations between layers may be independent!
- Accurate physical modeling of variations is nonexistent.
- How can one model coma aberrations on M3 and defocus on M4?

Complementary Design Solution: Process Variation Net Scanning (PVNS)

Modeling Lithographic Nonidealities

- **Perform a SPLAT simulation at every Pattern Match location and calculate changes in linewidth.**

Initial Results: Modeling CD Changes

- **Initial results show general trend from automated simulations and CD measurements.**
- **Outliers need to be rechecked for accuracy.**
- Fitted curves allow for a fast method to approximate response of CD to different aberrations using Pattern Matching.

Modeling Changes in Parasitics

Netlist Backannotation

- **At every net along the critical path, calculated changes in capacitance are lumped together at that node.**
- Effective resistance on the critical net is affected by resistances on and off the critical path.

Implementation using SVD Design

Future Goals

- Revalidation of process variation modeling through Pattern Matching and SPLAT simulations.
- Modeling of additional process variations (etch, CMP) using PVNS approach.
- Enhancements to the Pattern Matcher to match at certain locations and disable output filtering of matches.
- Comparison of Pattern Matching estimates of interconnect delay variation with brute force modeling.